Design Issues for a 50W VHF/UHF Solid State RF Power Amplifier

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thanks WWROF (wwrof.org)

Who Is K9LA?

- First licensed in October 1961 as WN9AVT
  - Selected K9LA in 1977
- Enjoy propagation, DX, contests, antennas, vintage rigs
- RF design engineer by profession (mostly RF power amplifiers)
  - BSEE 1969 and MSEE 1972 from Purdue University
  - Motorola Land Mobile 1974 to 1988 (Schaumburg and Fort Worth)
    - FM Power Amplifiers from 30 MHz to 512 MHz at 30 W to 100 W
    - Patent US4251784 Apparatus for Parallel Combining An Odd Number of Semiconductor Devices
  - Raytheon (formerly Magnavox) 1988 to Oct 2013 (Fort Wayne)
    - Power Amplifiers from 30 MHz to 2 GHz and from 10 W to 1 KW
    - Constant envelope waveforms (for example, FM) and non-constant envelope waveforms (for example, OFDM)
    - Patent 20040100341 MEMS-Tuned High-Power High-Efficiency Wide-Bandwidth Power Amplifier

Introduction

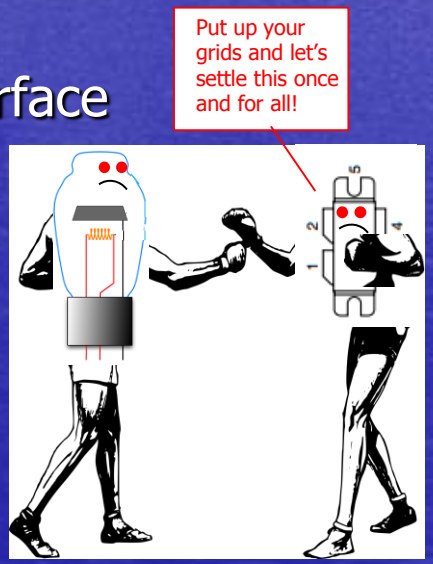
- A linear RF power amplifier (PA) takes a little signal and makes it bigger without losing fidelity

  theoretically!

- This presentation discusses several design issues for a very broadband 50 Watt power amplifier
- This presentation is not a construction project
- This presentation does not discuss all the issues tied to RF power amplifier design
  - There are books that do this
    - Cripps, Kenington, Dye & Granberg, etc

My Work With Transistors

- 1974-1988: BJTs (bipolar junction transistors)
  - My early days at Motorola – wow, 6 dB gain at 450 MHz!
- 1988-2000: Vertical MOS (metal oxide semiconductors)
- 2000-2010: Lateral MOS (LDMOS)
  - More gain than Vertical MOS, better thermal interface
  - About $1/watt when I retired in October 2013
- 2010-2013: GaN (gallium nitride)
  - Less dispersion of output parameters vs freq
    - Easier to match over wide range of frequencies
  - Depletion mode – need negative gate voltage
    - Voltage sequencing required
  - About $4/watt when I retired in October 2013
- Summary for my designs
  - LDMOS in PAs below 1 GHz and narrow band PAs up to 2 GHz
  - GaN for wideband PAs from 30 MHz to 2 GHz



Broadband Design

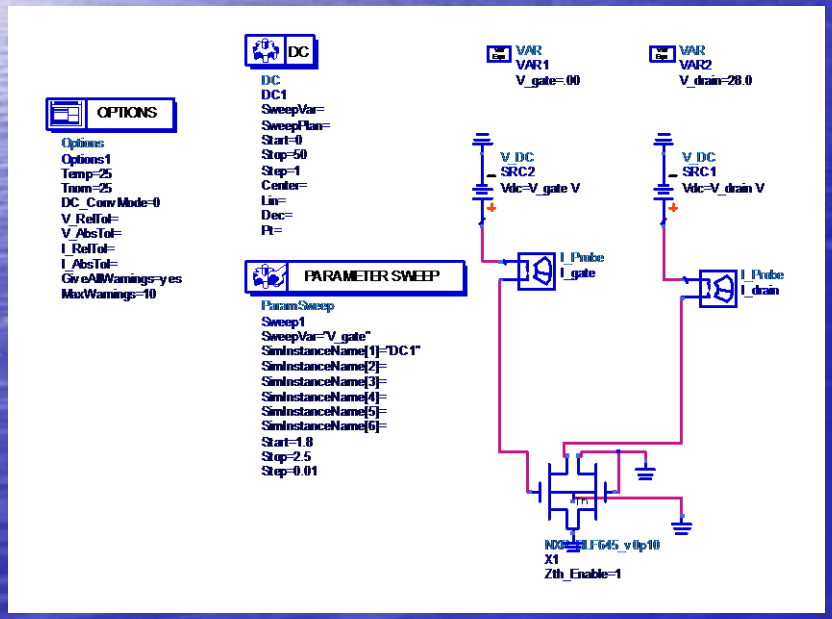
- Let's look at a 50 W PA from low VHF thru high UHF for a multitude of waveforms
  - 50 W means 50 W PEP (Peak Envelope Power) capability
    - 50 W continuous (slow CW) if heat sink and power supply are adequate
    - 50 W PEP for SSB
    - 12.5 W carrier for AM (AM peak-to-carrier ratio = 6 dB)
- Use a BLF645 push-pull LDMOS transistor
  - From NXP (formerly Philips)
- Suitable for 6m, 2m, 1.25m, 70cm and 33cm amateur bands (50 – 928 MHz)

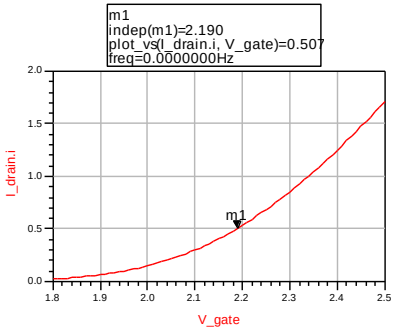
Design Decisions

- Idq
  - Class AB for decent linearity (for non-constant envelope waveforms) with reasonable efficiency
  - How far into Class AB?
    - Other classes (A, B, C, D, E, F, F^{-1}, S, etc) – not addressed
- Drain-to-gate feedback
  - Reduce gain at low-frequencies for improved stability
  - Reduce dispersion of Z_{in}
  - Flatten gain across operating bandwidth
- Desired load impedance
  - To meet output power, efficiency and linearity goals

Idq from ADS

- Use Agilent's ADS (Advanced Design System) to simulate Id vs Vg



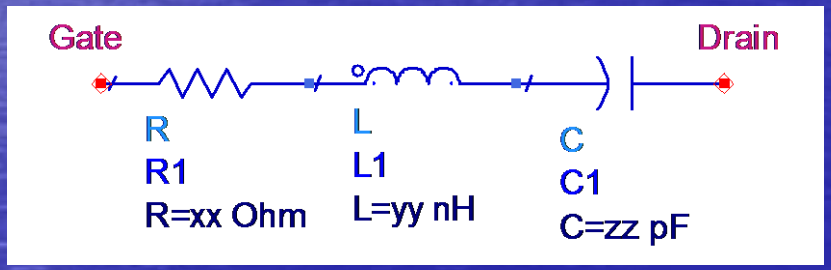


each side of the push-pull transistor

V_gate	I_drain.i freq=0.000	
1.800	21.34 mA	
1.810	24.14 mA	
1.820	27.23 mA	
1.830	30.61 mA	
1.840	34.30 mA	
1.850	38.30 mA	
1.860	42.62 mA	
1.870	47.27 mA	
1.880	52.28 mA	
1.890	57.65 mA	
1.900	63.40 mA	
1.910	69.57 mA	
1.920	76.17 mA	
1.930	83.24 mA	
1.940	90.80 mA	light AB
1.950	98.87 mA	
1.960	107.5 mA	
1.970	116.7 mA	
1.980	126.5 mA	
1.990	136.9 mA	
2.000	148.0 mA	
2.010	159.8 mA	
2.020	172.2 mA	
2.030	185.4 mA	
2.040	199.4 mA	
2.050	214.0 mA	
2.060	229.5 mA	
2.070	245.7 mA	
2.080	262.8 mA	
2.090	280.7 mA	
2.100	299.4 mA	
2.110	319.0 mA	
2.120	339.4 mA	
2.130	360.7 mA	
2.140	382.8 mA	
2.150	405.9 mA	
2.160	429.8 mA	
2.170	454.5 mA	
2.180	480.2 mA	medium AB
2.190	506.7 mA	
2.200	534.0 mA	
2.210	562.3 mA	
2.220	591.4 mA	
2.230	621.3 mA	
2.240	652.1 mA	
2.250	683.7 mA	
2.260	716.1 mA	
2.270	749.4 mA	
2.280	783.4 mA	
2.290	818.3 mA	
2.300	853.9 mA	
2.310	890.2 mA	
2.320	927.4 mA	
2.330	965.2 mA	
2.340	1.004 A	
2.350	1.043 A	
2.360	1.083 A	
2.370	1.124 A	
2.380	1.165 A	
2.390	1.207 A	
2.400	1.250 A	
2.410	1.293 A	
2.420	1.337 A	
2.430	1.381 A	
2.440	1.426 A	
2.450	1.472 A	heavy AB
2.460	1.518 A	
2.470	1.565 A	
2.480	1.612 A	
2.490	1.659 A	
2.500	1.708 A	

Feedback

- I've always believed it's a good idea to use some feedback to improve low frequency stability
- I usually used drain-to-gate feedback

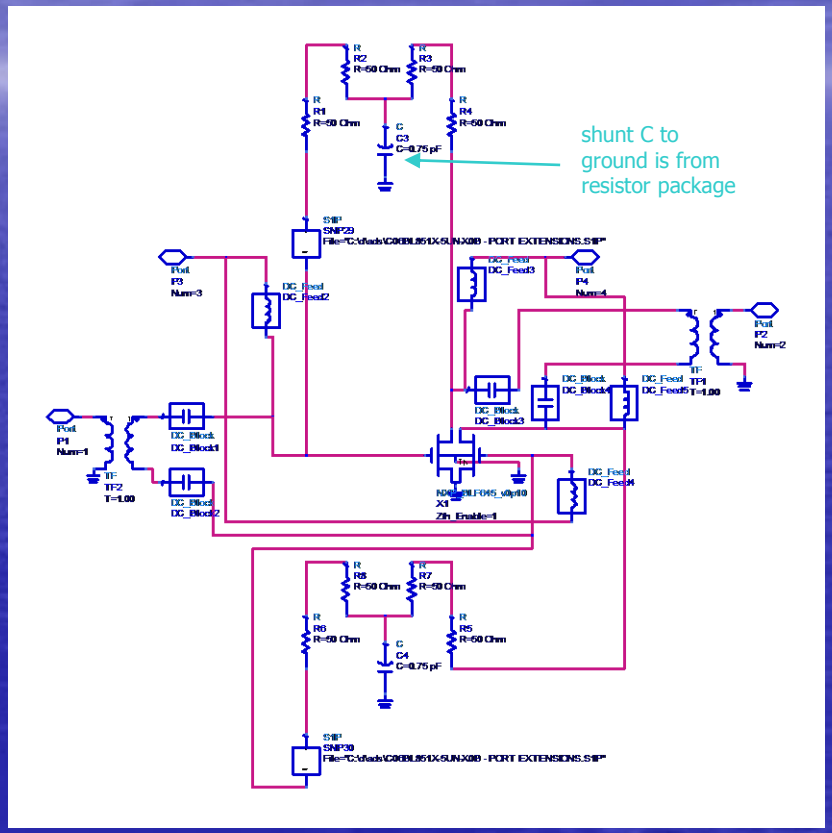


L1 is usually parasitic inductance from layout and parts themselves

- Sometimes need additional series R at gate or shunt R at gate for stability

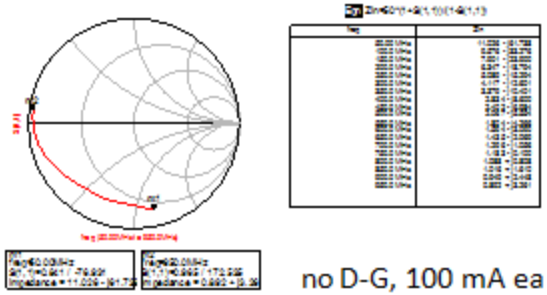
Input Impedance from ADS

- Going to be low
- Idq and feedback play important role
- Would like small dispersion of input impedance vs frequency
  - tight impedance arc
- Look at combinations of
  - Feedback R
    - none (infinite Ω), 800 Ω, 200 Ω
  - Idq (each side)
    - light AB (100 mA), medium AB (500 mA), heavy AB (1.5 A)



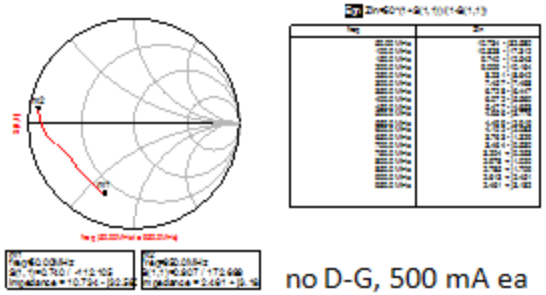
includes both sides of transistor and ideal 1:1 xfmrs

Each Side



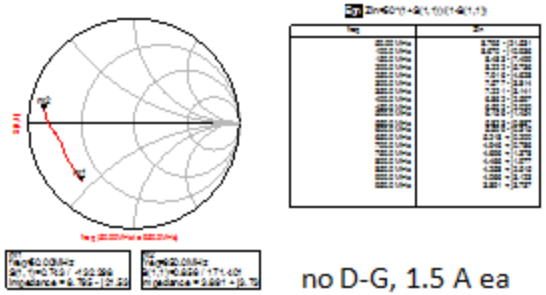
no D-G, 100 mA ea

Each Side



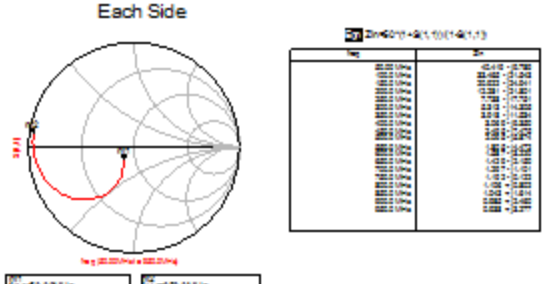
no D-G, 500 mA ea

Each Side



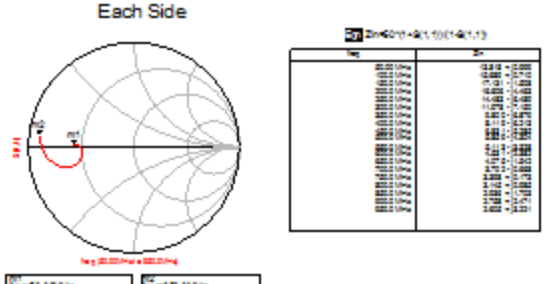
no D-G, 1.5 A ea

Each Side



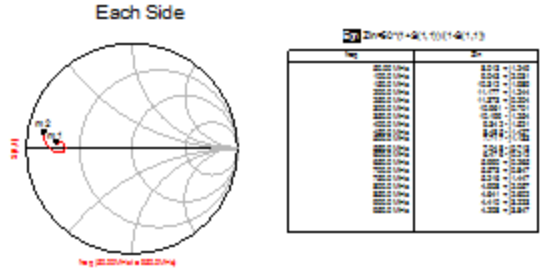
800 Ω, 100 mA ea

Each Side



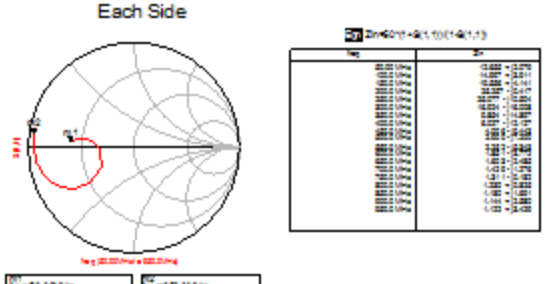
800 Ω, 500 mA ea

Each Side



800 Ω, 1.5 A ea

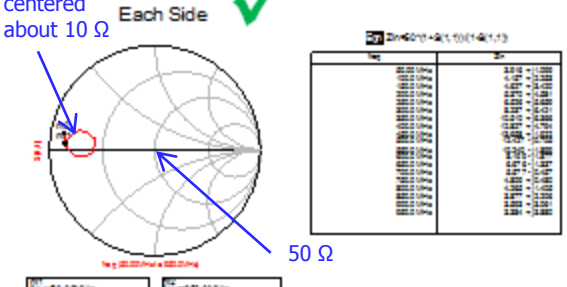
Each Side



200 Ω, 100 mA ea

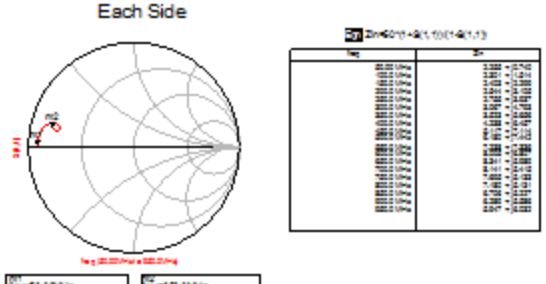
centered about 10 Ω

Each Side



200 Ω, 500 mA ea

Each Side



200 Ω, 1.5 A ea

Caveat on Input Impedances

- They are s-parameters
  - Gates driven with small signal
- BLF645 load impedance set to 50 Ω each side
  - 100 Ω drain-to-drain
  - Actual desired load ~ $V^2/(2 \times Pout)$ = 13 Ω each side = 26 Ω drain-to-drain (at low frequencies)
- Output load impedance affects input impedance
- When bias BLF645 to ~ 3 A drain current (emulating large signal) and terminate BLF645 with 26 Ω drain-to-drain, 'large signal' input impedances are very similar to 'small signal' input impedances
  - Sometimes two "wrongs" make a "right" !

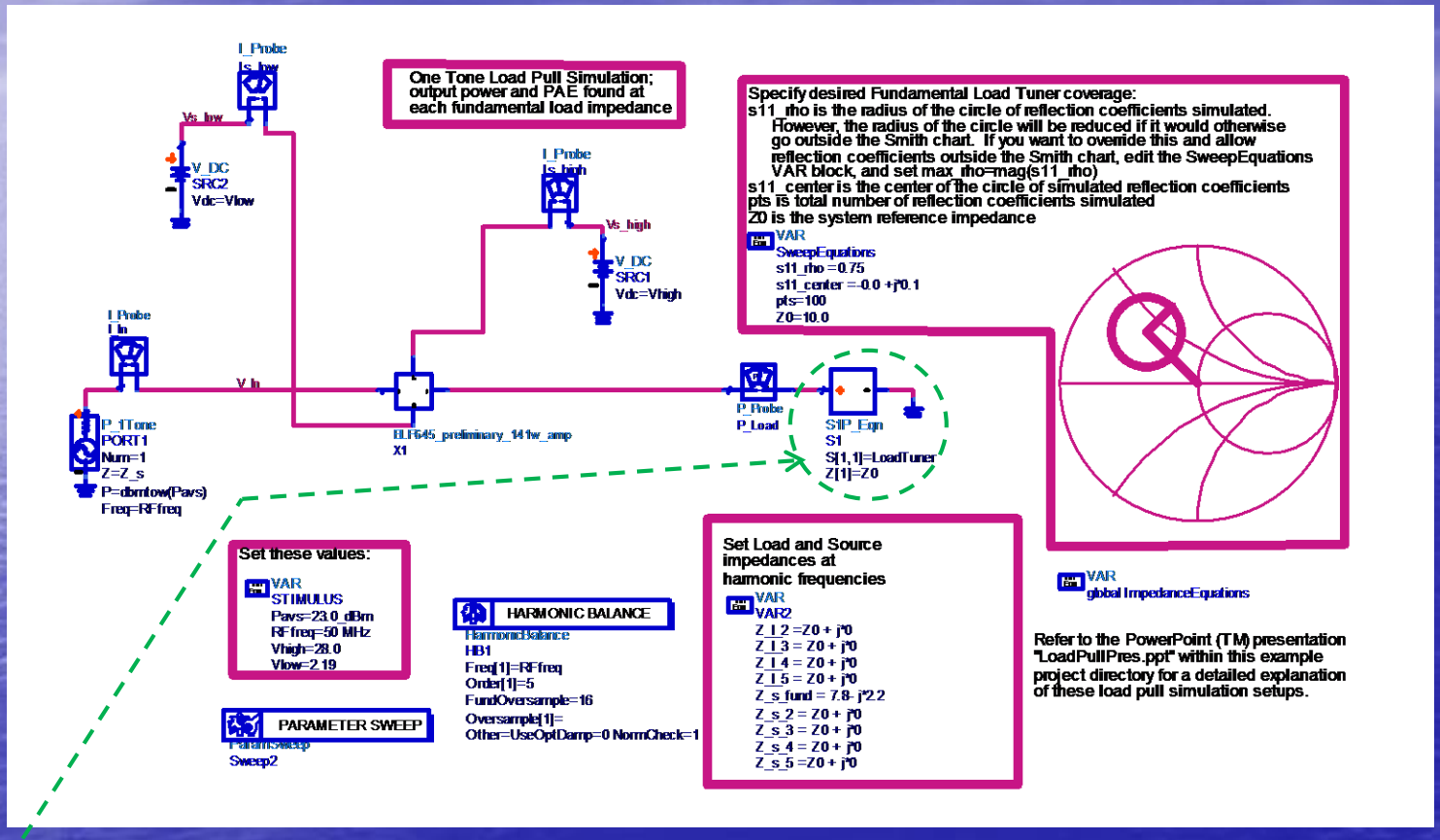
Input Network Design

- For 200 Ω feedback and 500 mA Idq each side
  - Z_{in} vs Frequency centered around 10 Ω
- 4:1 transformer is a good starting point
  - Don't put right at the body of the transistor
    - Use a little bit of series L (in conjunction with shunt C) to step up the BLF645 input impedance at the higher frequencies
      - BLF645 Z_{in} decreases with increasing frequency

Output Network Design

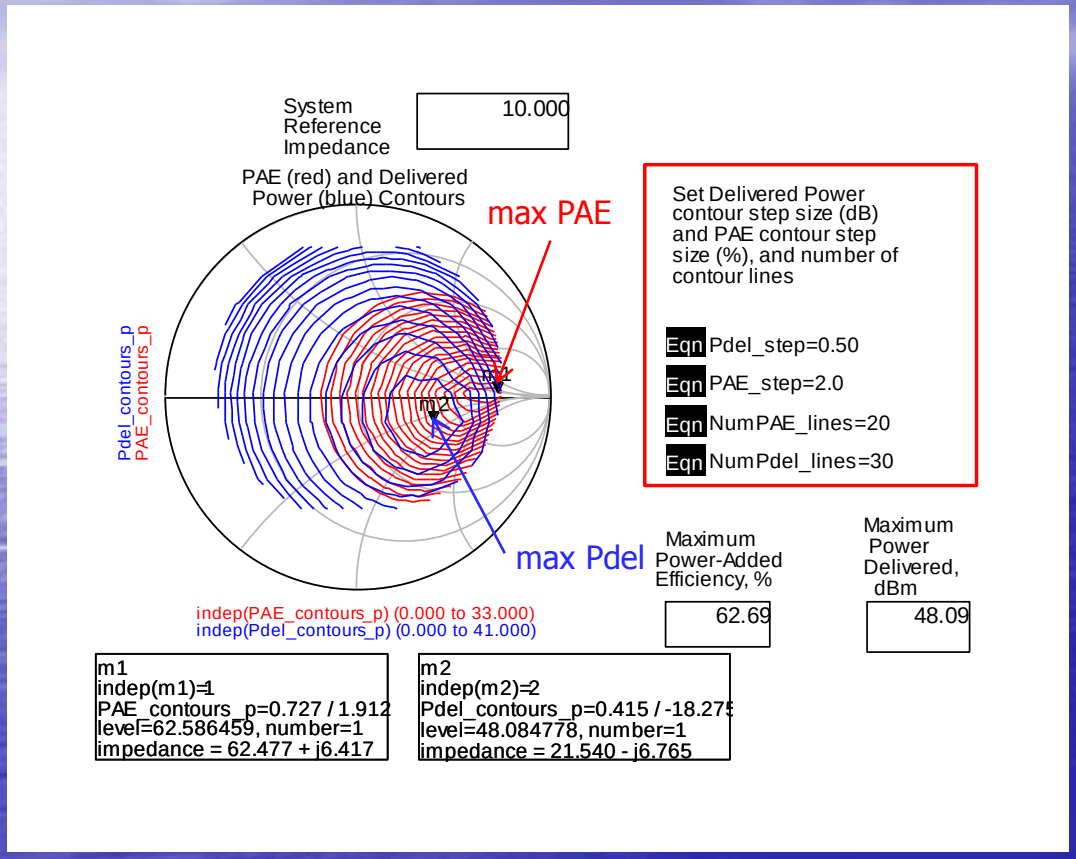
- What load impedance does the BLF645 want to see to meet output power, efficiency and linearity goals?
- Do load-pull in ADS with 200 Ω feedback and Idq = 500 mA (each side)
- Definitions
  - Pdel is power delivered to load (in dBm)
  - PAE is power added efficiency (in %)
    - $PAE = \frac{Pdel - Pin}{Vd \times Id} \times 100$

ADS Load-Pull



LoadTuner varies impedances over desired range while recording Pdel and PAE

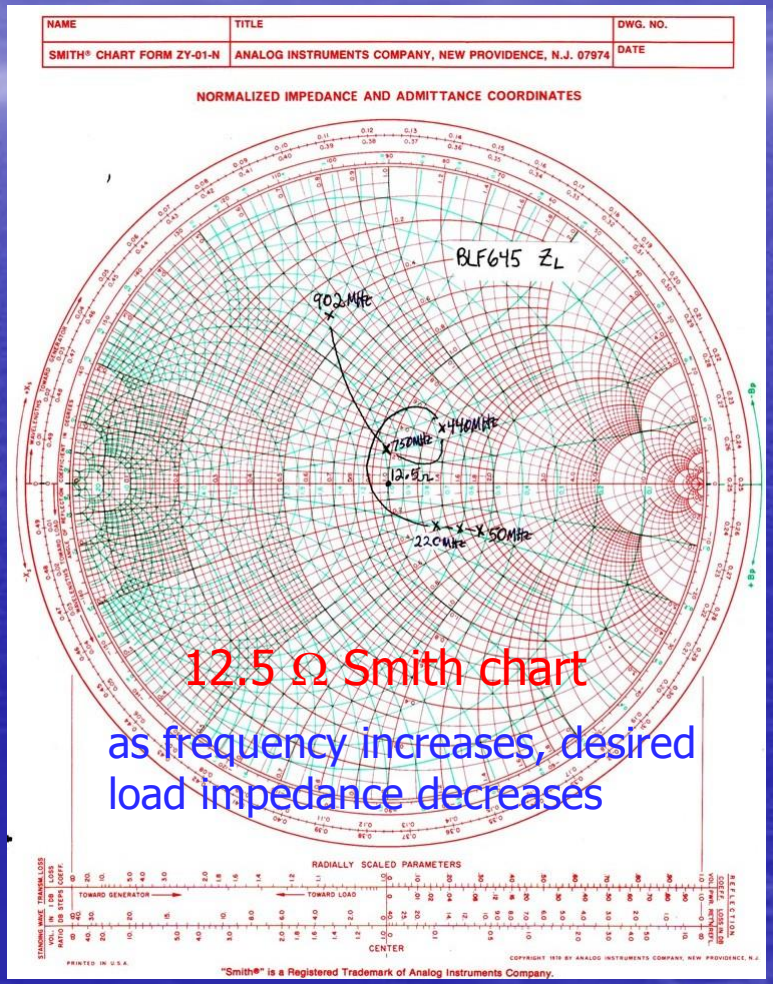
PAE/Pdel Data



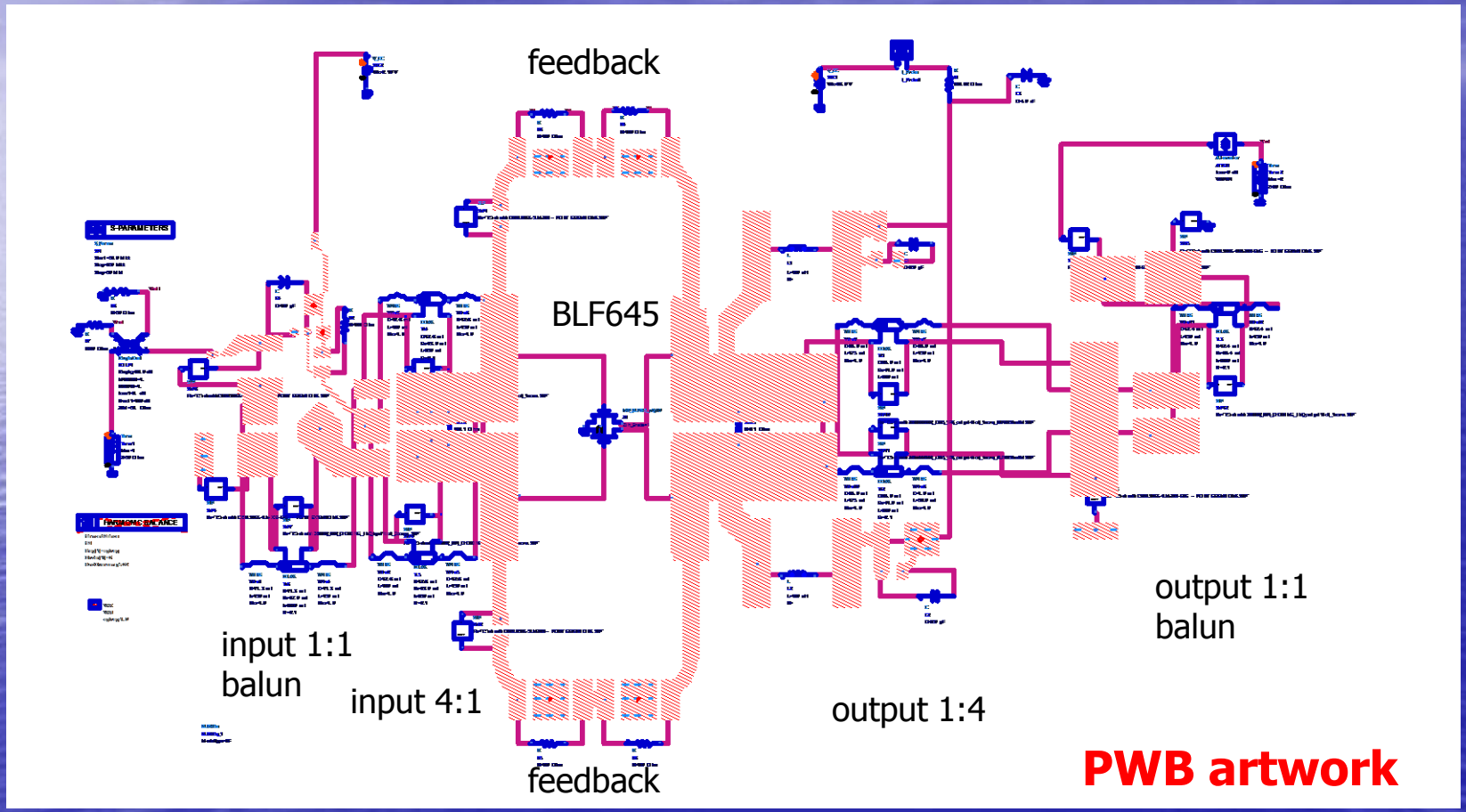
- Frequency is 50 MHz
- Pin = +23 dBm
- Z_o of Smith chart is 10 Ω
- Max Pdel is +48.09 dBm
- Max PAE is 62.69%
- Max Pdel and PAE usually don't occur at the same load impedance
- Decision – design for max Pdel
  - $Z_{desired\ load}$ = 21.5 – j 6.8 Ω
- PAE at max Pdel ~ 50%
- Pdel at max PAE ~ 45 dBm

Desired Z_{load} vs Frequency

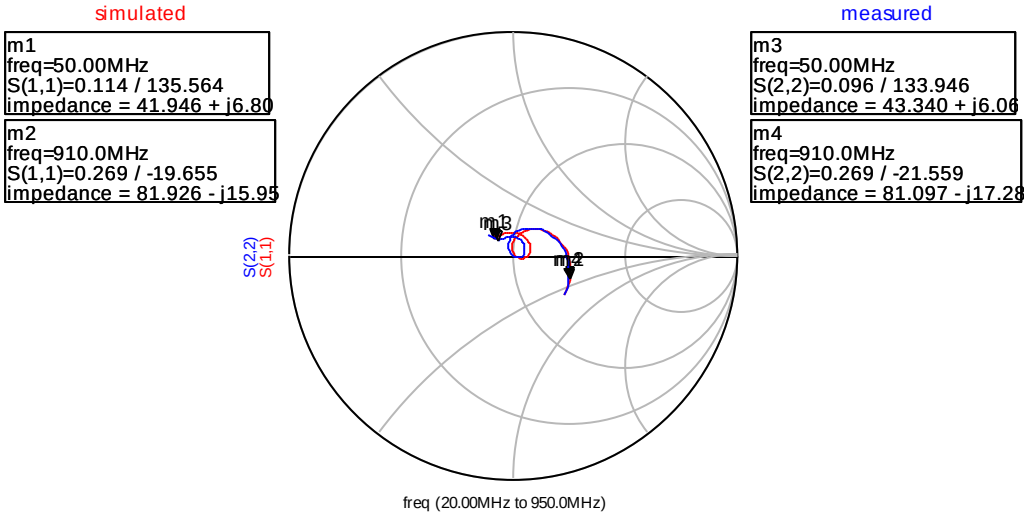
- Do load-pull at other frequencies
  - 50 MHz 21.5 – j 6.8 Ω
  - 145 MHz 19.2 – j 5.6 Ω
  - 220 MHz 16.8 – j 4.4 Ω
  - 440 MHz 16.5 + j 6.0 Ω
  - 750 MHz 11.8 + j 3.2 Ω
  - 902 MHz 5.0 + j 8.0 Ω
- All impedances are drain-to-drain
  - Plotted on 12.5 Ω Smith chart
- Desired load mostly around 12.5 Ω
  - Suggests 4:1 xfmr
- Using simple formula, we estimated 26 Ω at low frequencies
  - That's about where 50 MHz is



ADS Model: PWB and Schematic



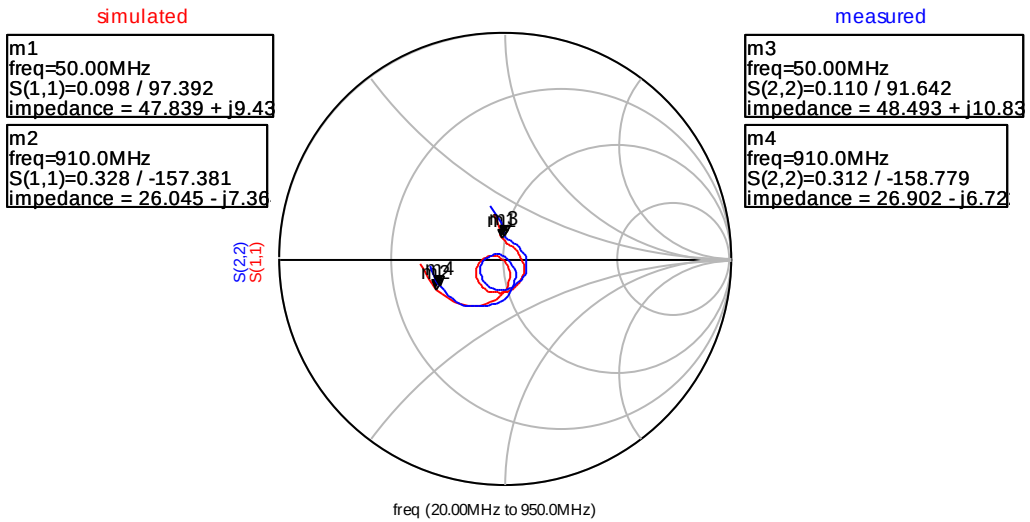
PWB + Schematic: Input



Looking into input RF connector with 12.4Ω gate-to-gate chip resistor substituted for BLF645

excellent correlation

PWB + Schematic: Output

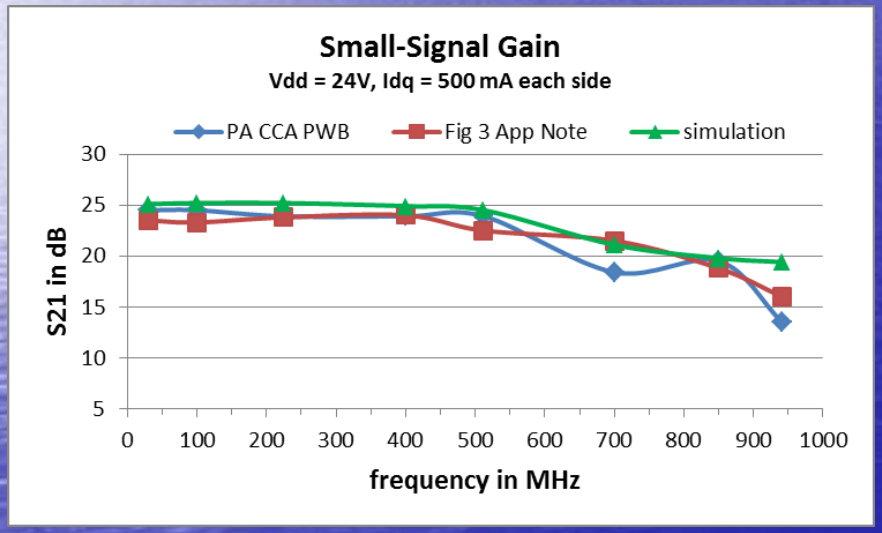


Looking into output RF connector with 12.4Ω drain-to-drain chip resistor substituted for BLF645

excellent correlation

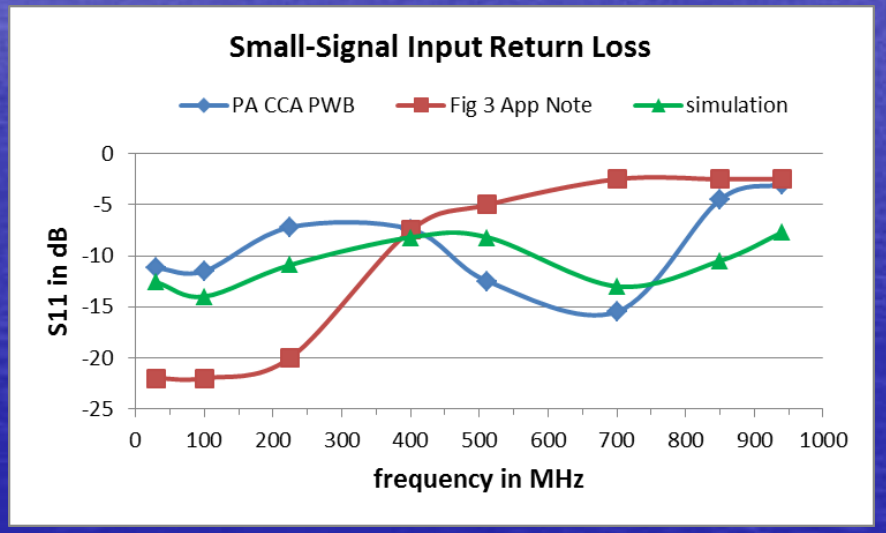
Small-Signal Comparison Simulated vs Measured

S21



good correlation overall

S11

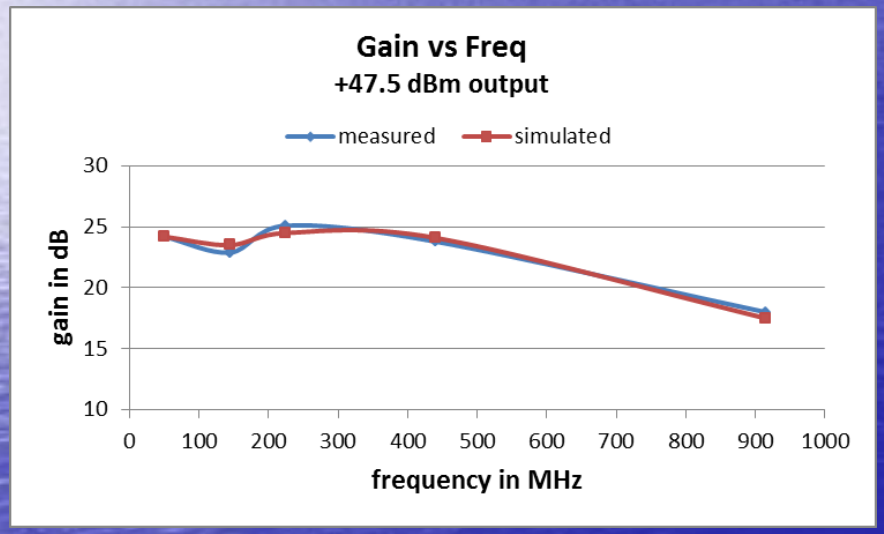


decent correlation between 'PA CCA PWB' and 'Simulation'

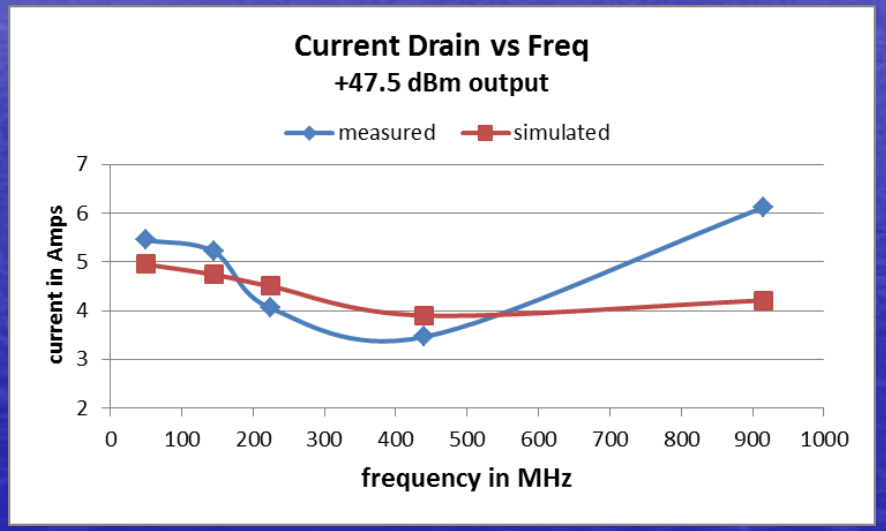
'PA CCA PWB' is measured breadboard
'Fig 3 App Note' is data from NXP app note
'Simulation' is from ADS model

Large-Signal Comparison Simulated vs Measured

at 28V



excellent correlation



decent correlation

'Measured' is the breadboard
'Simulation' is from ADS model

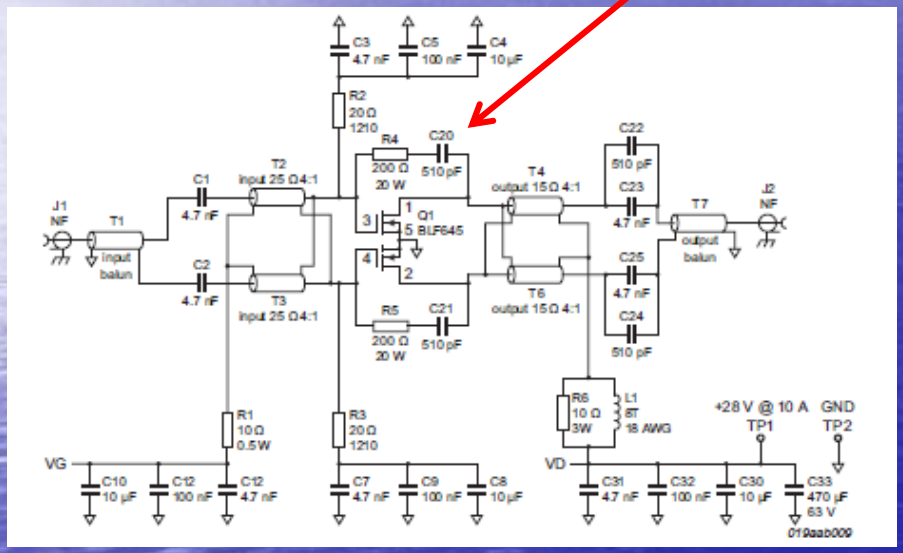
Large-Signal Performance Measured Data

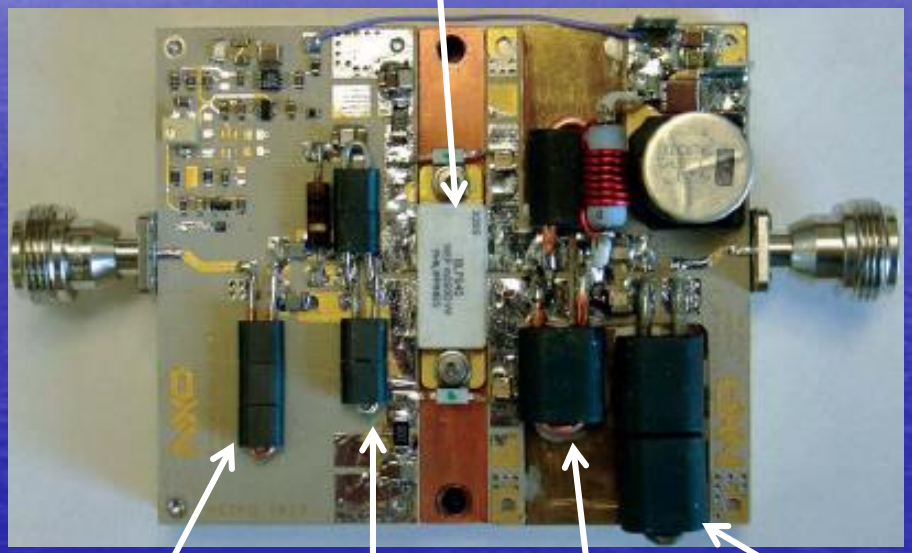
at 28V

freq	Pout	Pin	Gain	Current	Eff	2f	3f	Input RL
50 MHz	47.5 dBm	23.3 dBm	24.2 dB	5.45 A	36.8%	-43 dBc	-13 dBc	12.2 dB
145	47.5	24.6	22.9	5.21	38.5	-64	-14	7.5
225	47.5	22.4	25.1	4.05	49.6	-36	-17	9.0
440	47.5	23.7	23.8	3.46	58.0	-54	-26	8.2
915	47.5	29.5	18.0	6.12	32.8	-38	-45	14.4

this is the breadboard

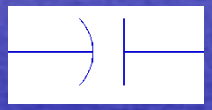
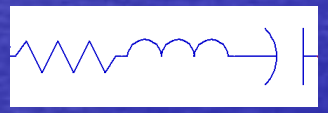
BLF645 Design Implementation





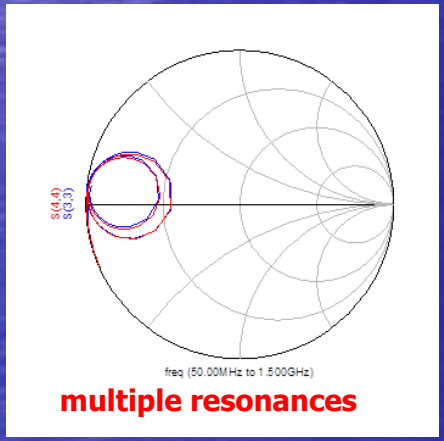
schematic and breadboard photo from NXP App Note AN10953

Caveat On Simulation

- Simulation results are only as good as the models used
- Chip capacitor example – 300 pF ATC 100B (100 mil cube)
  - Very simple model – series C 
  - Better model – series RLC  R=0.1 Ω, L=0.5 nH
  - Best model – from network analyzer measurement of cap

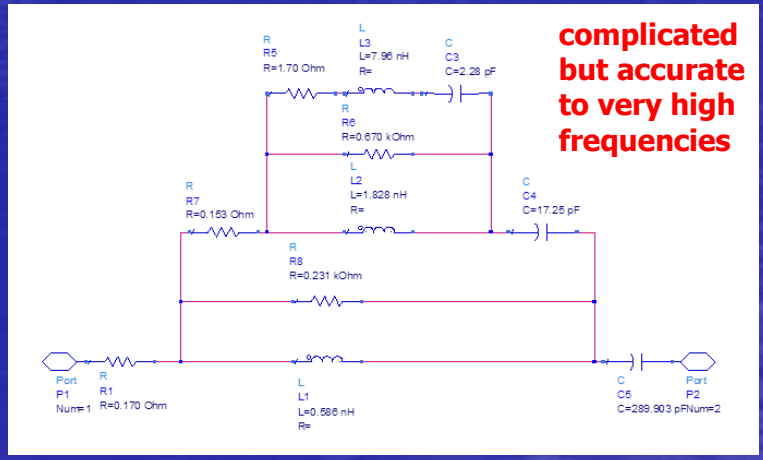
blue is measured

red is simulated



multiple resonances

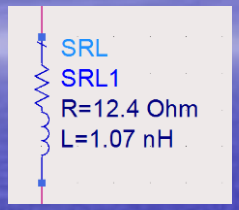
both images from Mark Walker KB9TAF presentation at an inter-company RF symposium



complicated but accurate to very high frequencies

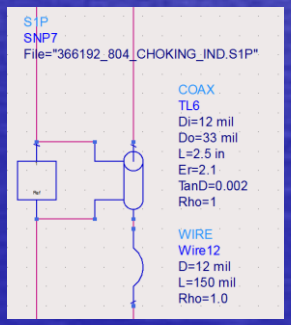
Other Components, and IMD

- Resistors
  - Series R-L is usually sufficient
  - Generally not in the RF path



0805 chip resistor
X_L about 6 ohms at 900 MHz

- Inductors
  - Might be some inter-winding capacitance at the higher frequencies
- RF transformers
  - Used transmission-line transformers (TLT)
  - Modeled with a length of coax
  - Impact of ferrite modeled as inductance of outer conductor
    - S-parameter measurement – we called it 'magnetizing inductance'



1:1 balun

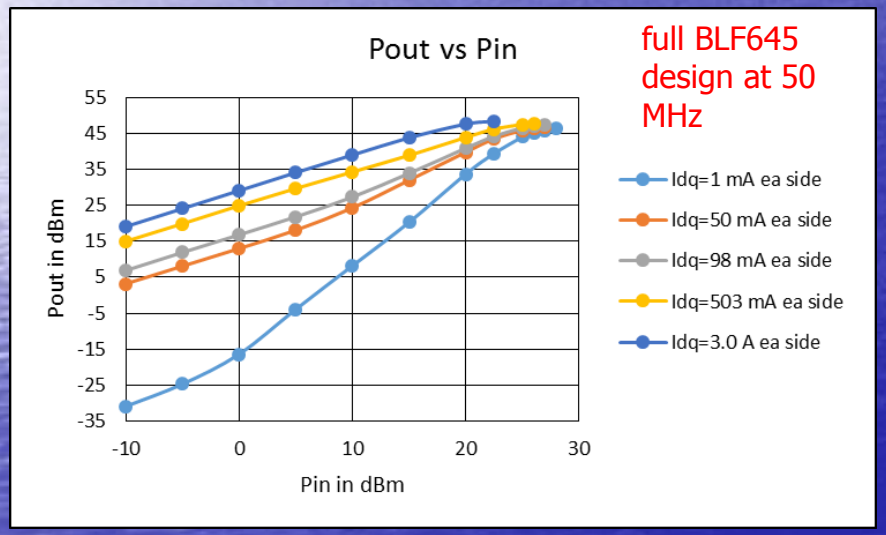
- Simulating IMD
  - Areas of concern: transistor model, impact of ferrite on xfmrs
  - Use results cautiously - rule of thumb for medium Class AB – if PEP of waveform is at P1dB, 2-tone IMD ~ -25 dBc or AM distortion ~ 5%

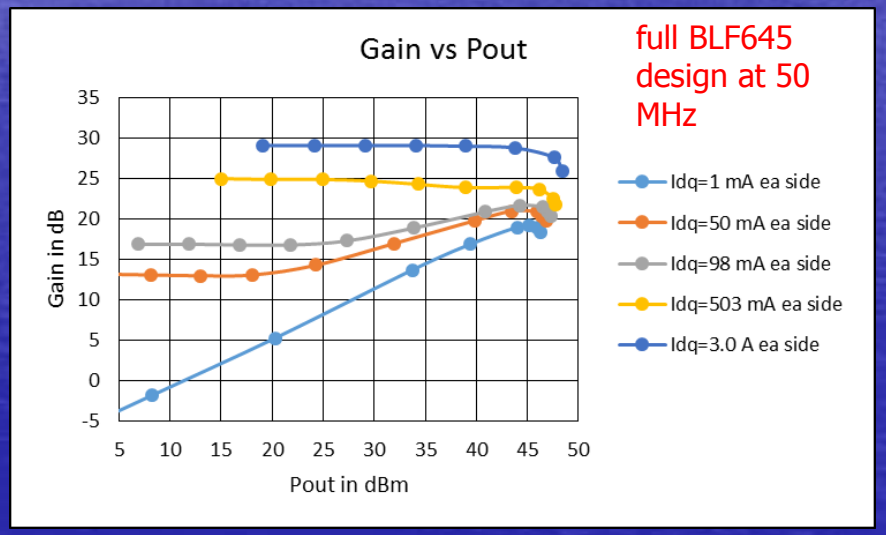
More Simulation Comments

- What if you don't have simulation capabilities?
  - Design the old-fashioned way
    - Start with data sheet impedances
    - Play around on the bench a lot – as Ed Paragi WB9RMA and I did in our early PA design days
- Simulation allows you to look at many "what if" scenarios in a short amount of time
- The model can be used for trends, and if it's good enough it can be used for absolute results (usually the model of the transistor is the limiting factor)

Simple Characterization of a PA

- The November 2015 QST had a Product Review of a 6m amplifier – showed a plot of Pout vs Pin
- Better way to characterize a PA – plot Gain vs Pout





- Gain vs Pout tells class of operation (flat gain is A or medium/high AB), tells gain (from plot), shows compression, and indicates efficiency (A is least efficient)
- Gain vs Pout indicates linearity (flat gain best, gain expansion not good)

Summary

- Discussed design issues for a broadband VHF/UHF PA
- More work needed for complete design
  - P_{in} from 0.2 – 1.0 W: could add gain compensation
  - Power supply: 28 V at 7 A
  - Heat sink: max dissipation = 120 W *need to get the heat out!*
  - 5 harmonic filters: push-pull eases 2f rejection (see slide 22)
  - T/R Switch: relays easiest, could use PIN diodes
  - Directional coupler on output: P_{fwd} and P_{refl} , use P_{fwd} for ALC
- Harmonic filters, T/R Sw and dir cplr add loss
- Simulation is a big help, but bench performance determines success or failure
  - Accurate models give accurate simulations
- Thanks to WB9RMA and KB9TAF for comments to these slides